

1.1 What do you mean by pipelining? Represent the 5 stage pipeline execution of the instructions

```
lw $10 20($1)
sub $11 $2 $3
```

1.2 Illustrate the 5 stage pipeline execution of instructions

```
add $10 $1 $2
sub $3 $10 $4
```

2. Illustrate the 5 stage pipeline execution of instructions

```
lw $2 20($1)
sub $4 $2 $3
```

3. Show the pipeline execution of following program.

```
sub    $2, $1, $3
and    $12, $2, $5
or     $13, $6, $2
add    $14, $2, $2
sw     $15, 100($2)
```

4. Show how to improve the performance of following code sequences.

```
4.1
Add $4 $5 $6
Beq $1 $2 40
Lw $3 300($0)
```

```
4.2
Lw $t0 0($t1)
Lw $t2 4($t1)
Sw $t2 0($t1)
Sw $t0 4($t1)
```

5. Identify the control signals transmitted from the main controller of the single cycle processor to each pipeline register for R-type, lw/sw, beq and J instructions.

6.

Illustrate the pipelined data path and control path to improve performance of single cycle MIPS processor that implements R-type, lw/sw, beq and J instructions. Identify each pipeline register by the name of the field value that is to be loaded, length of the field and total length of the pipeline register.

7. Instruction Decode, ID, stage of the pipeline processor receives following instruction bits:

Bits 15-0 = 2090

20-16 = 11

15-11 = 1

26-21 = 10

Control unit in the ID stage produces 1100 000 10 for EX, MEM and WB stages. Identify the instruction.

8. Execution stage of the pipeline processor receives following instruction bits:

Bits 15-0 = 16

20-16 = 6

15-11 = 0

26-21 = 5

Control signals for the EX, MEM and WB stages of the execution stage are 0001 001 00. Identify the instruction.

9. Show the following code going through the pipeline.

```
Lw $10 20($1)
Sub $11 $2 $3
And $12 $4 $5
Or $13 $6 $7
Add $14 $8 $9
```

10. Design the forwarding unit for single cycle pipeline processor.